R E M A R K S

Reconsideration of this application, as amended, is respectfully requested.

RE: THE CLAIM AMENDMENTS

Claim 1 has been amended to clarify the features of the present invention whereby in the semiconductor construction assembly, columnar electrodes are formed on the pads of the conductors, and a sealing film is formed between the columnar electrodes and on the protective layer, as supported by the disclosure in the specification at, for example, page 18, line 24 to page 19, line 10. And claim 1 has also been amended to clarify the feature of the present invention whereby the upper insulating layer covers the semiconductor construction assembly and the sealing member except for portions corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes, as supported by the disclosure in the specification at, for example, page 20, lines 7-20.

In addition, claim 22 has been amended to clarify the features of the present invention whereby the semiconductor construction assembly includes projecting electrodes which are coupled to pads of a semiconductor substrate and which have substantially flat respective upper surfaces, and a sealing member which is formed between the projecting electrodes

and covers an upper surface of the semiconductor substrate while externally exposing at least the upper surfaces of the projecting electrodes such that the substantially flat upper surfaces of the projecting electrodes and an upper surface of the sealing member are substantially flush with each other, as supported by the disclosure in the specification at, for example, page 18, line 24 to page 19, line 10.

Still further, claim 23 has been amended to clarify the features of the present invention whereby each of the semiconductor construction assemblies are separately arranged from each other, and each includes projecting electrodes which are coupled to pads of a semiconductor substrate and which have flat respective upper surfaces, and an organic insulating film which is formed between the projecting electrodes and covers an upper surface of the semiconductor substrate while externally exposing at least the upper surfaces of the projecting electrodes such that the substantially flat upper surfaces of the projecting electrodes and an upper surface of the organic insulating film are substantially flush with each other, as supported by the disclosure in the specification at, for example, page 18, line 24 to page 19, line 10. In addition, claim 23 has also been amended to clarify the feature of the present invention whereby the sealing member is formed at least in a gap adjacent to the semiconductor construction assemblies, as supported by the

disclosure in the specification at, for example, page 19, line 25 to page 20, line 6. And claim 23 has also been amended to clarify the feature of the present invention whereby the upper insulating layer covers one entire surface of the semiconductor construction assemblies and at least a portion of the sealing member, as supported by the disclosure in the specification at, for example, page 20, lines 7-11.

Yet still further, claims 1, 3-5, 11-13, 15-20, 22 and 23 have been amended to make some minor grammatical improvements and to correct some minor antecedent basis problems so as to put them in better form for issuance in a U.S. patent. The informalities pointed out by the Examiner in claims 3 and 13 have been corrected, and it is respectfully submitted that all of the claims fully comply with the requirements of 35 USC 112, second paragraph.

Finally, claims 39 and 40 have been added depending from claims 22 and 23 to recite the feature of the present invention whereby the projecting electrodes are formed from a same material as the upper conductor.

No new matter has been added, and it is respectfully requested that the amendments to claims 1, 3-5, 11-13, 15-20, 22 and 23 and the addition of claims 39 and 40 be approved and entered, and that the rejection under 35 USC 112, second paragraph, be withdrawn.

RE: WITHDRAWAL OF CLAIM 23 FROM CONSIDERATION

The Examiner has withdrawn claim 23 from consideration on the grounds that the organic insulating layer recited in claim 23 is different from the insulating layer of an inorganic material recited in claim 3, which depends from claim 1.

It is respectfully pointed out that the organic insulating layer recited in claim 23 is a completely different structure from the insulating layer of an inorganic material recited in claim 3, and it is respectfully submitted that the recitation of an organic material from claim 3 does not exclude claim 23 from the species of claim 1.

More specifically, according to amended claim 3, an additional insulating layer made of an inorganic material is formed between the semiconductor substrate and the protective layer of the semiconductor construction assembly. And according to amended independent claim 1, from which claim 3 depends, a sealing film is formed on the protective layer and between the columnar electrodes.

Claim 23, on the other hand, recites an organic insulating film which is formed between the projecting electrodes and covers an upper surface of the semiconductor substrate.

That is, the organic insulating film of claim 23 is analogous to the sealing film of claim 1, not the insulating layer of claim 3. And it is respectfully submitted that the

explicit recitation that the insulating film of claim 23 is organic does not render claim 23 to be a different species from claim 1. Indeed, as explained in the paragraph bridging pages 18 and 19 of the specification "A sealing film (insulating film) 33 made of an epoxy resin or the like is formed on the upper surface of the protective film." That is, the sealing film of claim 1 may be an epoxy (hence, organic) resin, just like the organic insulating film of claim 23.

In view of the foregoing, it is respectfully requested that the withdrawal of claim 23 from consideration be reconsidered, and that claim 23 be considered on the merits along with the other elected claims, 1-17 and 22.

RE: WITHDRAWN CLAIMS 18-20

It is respectfully requested that withdrawn claims 18-20 also be considered on the merits and allowed upon allowance of elected claims 15 and 1 from which claims 18-20 depend.

RE: THE PRIOR ART REJECTION

Claims 1, 2, 4, 5-9, 11-17 and 22 were rejected under 35 USC 102 or under 35 USC 103 as being anticipated by or obvious in view of USP 6,154,366 ("Ma et al"), and claims 3 and 10 were rejected under 35 UCS 103 as being obvious in view of the combination of Ma et al and US 2003/0133274 ("Chen et al").

These rejections, however, are respectfully traversed with respect to the claims as amended hereinabove.

According to the present invention as recited in amended claim 1, a semiconductor device is provided which comprises a semiconductor construction assembly that includes: (i) a semiconductor substrate having first and second surfaces that are mutually opposed to each other, and a plurality of side surfaces between the first surface and the second surface, (ii) an integrated circuit element formed on the first surface, (iii) a plurality of connection pads which are arranged on the first surface and connected to the integrated circuit element, (iv) a protective layer which is formed to cover the first surface of the semiconductor substrate and which has openings for exposing the connection pads, (v) a plurality of conductors which are connected to the connection pads and arranged on the protective layer and which have pads, (vi) columnar electrodes formed on the pads of the conductors, and (vii) a sealing film formed between the columnar electrodes and on the protective layer. A sealing member covers at least one side surface of the semiconductor construction assembly. An upper insulating layer covers the semiconductor construction assembly and the sealing member except for portions corresponding to the columnar electrodes so as to expose an upper surface of each of the columnar electrodes. Upper conductors are formed on the upper insulating layer, and

each of the upper conductors includes one end that is electrically connected to the pad of one of the conductors via one of the columnar electrodes and at least one external connection pad. And an external connection pad of at least one of the upper conductors is disposed in a region opposing the sealing member.

It is respectfully pointed out that it is important to cover the surface of a semiconductor chip (including a semiconductor substrate having an integrated circuit) having connection pads arranged by a minute pitch, and to form, on the resin covering the semiconductor chip, an external terminal which is connected to the connection pads and has a large area and a pitch larger than that of the connection pads of the semiconductor chip, so as to realize high-density packaging such that small electronic devices can have multiple functions while remaining compact.

Conventional semiconductor devices have encountered problems when covering the surface of the semiconductor chip with resin and forming a connection wiring thereon, such as the semiconductor chip being damaged, and the properties of the integrated circuit changing due to ion impurities in the resin.

For example, a common method of forming a resin on the semiconductor chip is thermally pressing the semiconductor chip and the resin. However, the strength of the semiconductor chip is usually not strong enough to endure thermal pressing, and the

connections between the connection pads and the connection wiring may be broken or short-circuited due to an impact or changes in the ambient environment when the semiconductor chip is moved (usually, the manufacturer or the location of the semiconductor chip is different from the manufacturer or the location of the semiconductor device). Even if disconnection does not occur, the state of the semiconductor chip may approach breakdown due to stress concentration. In particular, it is clear that in aging (temperature cycle test) before and after a process of forming the resin on the semiconductor chip, yield is low. In short, in a semiconductor device of this type, sufficient reliability is not ensured, and therefore this type of semiconductor has not been fully adopted by leading semiconductor manufacturers.

According to the present invention as recited in amended claim 1, therefore, the semiconductor construction assembly includes: a protective layer which covers the first surface of the semiconductor substrate in the semiconductor construction assembly, and which has openings for exposing the connection pads on the first surface of the semiconductor substrate; a plurality of conductors which are connected to the connection pads and arranged on the protective layer and which have pads; columnar electrodes formed on the pads of the conductors; and a sealing film formed between the columnar electrodes and on the protective layer.

With this structure, when forming the upper insulating layer of claim 1 on the semiconductor construction assembly by thermal pressing, the semiconductor construction assembly has enough strength to endure heating and pressing. More specifically, before the process of forming an upper surface wiring board, the semiconductor assembly is sufficiently protected by the sealing film that surrounds the columnar electrodes. In addition, the columnar electrodes are connected to the upper conductors, and the columnar electrodes have a function of absorbing stress concentration due to differences in temperature. Still further, the sealing film inhibits ion impurities from permeating into the integrated circuit. The semiconductor construction assembly according to claim 1 can therefore better withstand impact and can better endure change in the ambient environment when moved. As a result, the incidence of failure in aging is low.

By contrast, it is respectfully submitted that Ma et al does not disclose, teach or suggest columnar electrodes formed on the pads of conductors that are formed on a protective layer and connected to the connection pads of a semiconductor substrate, or a sealing film that is formed between the columnar electrodes and on the protective film, as recited in amended claim 1.

Indeed, although the Examiner has referred to Fig. 3k of Ma et al as disclosing columnar electrodes, it is respectfully submitted that no columnar electrodes are present therein.

If the Examiner considers that the bases of solder balls 156 of Ma et al are columnar electrodes, then it is respectfully pointed out that according to amended claim 1 in addition to the sealing film formed between the columnar electrodes, an upper insulating layer covers the semiconductor construction assembly (of which the columnar electrodes are a part) except for the exposed upper surfaces of the columnar electrodes. And it is respectfully pointed out that according to amended claim 1 the columnar electrodes serve to electrically connect conductors to upper conductors that are formed on the upper insulating layers and that include external connection pads.

Thus, it is respectfully submitted that Ma et al clearly does not disclose columnar electrodes and a sealing film in the manner of the claimed present invention as recited in amended claim 1.

According to the present invention as recited in amended independent claim 22, moreover, the semiconductor construction assembly of a semiconductor device includes projecting electrodes which are coupled to pads of a semiconductor substrate and which have substantially flat respective upper surfaces, and a sealing member which is formed between the projecting electrodes and covers an upper surface of the semiconductor substrate while externally exposing at least the upper surfaces of the projecting electrodes such that the substantially flat upper surfaces of the

projecting electrodes and an upper surface of the sealing member are substantially flush with each other.

Similarly, according to the present invention as recited in amended independent claim 23, each of a plurality of semiconductor construction assemblies, which are separately arranged from each other, includes projecting electrodes that are coupled to pads of a semiconductor substrate and have flat respective upper surfaces, and an organic insulating film which is formed between the projecting electrodes and covers an upper surface of the semiconductor substrate while externally exposing at least the upper surfaces of the projecting electrodes such that the substantially flat upper surfaces of the projecting electrodes and an upper surface of the organic insulating film are substantially flush with each other.

Thus, according to the present invention as recited in each of amended independent claims 22 and 23, in a semiconductor construction assembly, a projecting electrodes coupled to pads of a semiconductor substrate have a sealing film (or organic insulating film as recited in claim 23) formed therebetween, and the substantially flat upper surfaces of the projecting electrodes are flush with the upper surface of the sealing film (organic insulating film).

It is respectfully submitted that Ma et al does not disclose, teach or suggest these features of the present

invention as recited in amended independent claims 22 and 23, within the structure of the semiconductor devices of claims 22 and 23, wherein an upper insulating layer is provided over the semiconductor construction assembly and at least one upper conductor is formed on the upper insulating layer, electrically connected to the projecting electrode, and extends to a region corresponding to the second sealing member.

It is respectfully submitted, moreover, that Chen et al has merely been cited for the disclosure of the sealing member and the semiconductor construction assembly having lower surfaces that are substantially flush with each other and a buried member having substantially a same thickness as a thickness of the semiconductor construction assembly.

And it is respectfully submitted that Chen et al does not disclose, teach or even remotely suggest columnar electrodes and a sealing film as recited in amended claim 1. Indeed, it is respectfully submitted that Chen et al is directed to forming an insulation layer 320 and circuit layer 342 on a chip 400 to form one or more build-up circuit structurs 370 and does not at all disclose columnar electrodes with a sealing film (or organic insulating film as recited in claim 23) formed therebetween.

Accordingly, even if Chen et al were combinable with Ma et al in the manner suggested by the Examiner, it is respectfully submitted that the present invention as recited in amended

independent claims 1, 22 and 23 still would not be achieved or rendered obvious.

In view of the foregoing, it is respectfully submitted that amended independent claims 1, 22 and 23, as well as claims 3-5 and 8-20 depending from claim 1, and claims 39 and 40 depending from claims 22 and 23, all clearly patentably distinguish over Ma et al and Chen et al, taken singly or in combination, under 35 USC 102 as well as under 35 USC 103.

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Entry of this Amendment, allowance of the claims and the passing of this application to issue are respectfully solicited.

If the Examiner has any comments, questions, objections or recommendations, the Examiner is invited to telephone the undersigned at the telephone number given below for prompt action.

Respectfully submitted,

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